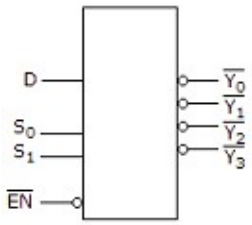
Department of Computer Science
Class: F. Y. B. Sc. (CS)
Semester: I
Subject: Digital System and Architecture
Sample Questions

Multiple Choice Questions

1. There are _____ cells in a 4-variable K-map.
    a. 12
    b. 18
    c. 8
    d. 16
2. The quantity of double word is _____
    a. 16 bits
    b. 32 bits
    c. 4 bits
    d. 8 bits
3. Which functional unit is used to store data or information
    a. input unit
    b. output unit
    c. memory
    d. bus structure
4. According to Boolean law: A + 1 = ?
    a. 1
    b. A
    c. 0
    d. A'
5. How many AND gates are required to realize Y = CD + EF + G?
    a. 4
    b. 5
    c. 3
    d. 2
6. The inverter is ……
    a. NOT gate
    b. OR gate
    c. AND gate
    d. NAND gate
7. An OR gate has 4 inputs. One input is high and the other three are low. The output is …….
    a. Low
    b. High
    c. alternately high and low
    d. may be high or low depending on relative magnitude of inputs
8. The result of 0*1 in binary is _____
    a. 0
    b. 1
    c. Invalid

d. 10

9. Four adjacent ‘1’s in a Karnaugh map forms a
    a. octet
    b. singlet
    c. pair
    d. quad
10. If n denotes the number of variable then the number of cells are given as
    a. 2^n
    b. 2 + n
    c. 2 – n
    d. 2n
11. In a Karnaugh map, a group of eight 1’s adjacent to each other is called
    a. Pairs
    b. Triad
    c. Quads
    d. Octet
12. In a Karnaugh map the formation of Quad results in the elimination of _____ variables and their complements.
    a. 2
    b. 3
    c. 4
    d. 8
13. The device shown here is most likely a _____



    a. Comparator
    b. Multiplexer
    c. Inverter
    d. Demultiplexer

14. 3 bits full adder contains _____
    a. 3 combinational inputs
    b. 4 combinational inputs
    c. 6 combinational inputs
    d. 8 combinational inputs
15. In a combinational circuit, each output depends entirely on the _____ inputs to the circuit.
    a. Same
    b. Different
    c. Common
    d. Immediate
16. Total number of inputs in a half adder is _____
    a. 2

b. 3
c. 4
d. 1

17. In which operation carry is obtained?
    a. addition
    b. subtraction
    c. Multiplication
    d. Division

18. In 1-to-4 demultiplexer, how many select lines are required?
    a. 2
    b. 3
    c. 4
    d. 5

19. In _____ counter different flip flops are triggered with different clock, not simultaneously.
    a. Asynchronous Counter
    b. Synchronous counter
    c. Up counter
    d. Down counter

20. In 4-bit up-down counter, how many flip-flops are required?
    a. 2
    b. 3
    c. 4
    d. 5

21. MU, ALU and CU are all part of the _____.
    a. Storage Memory
    b. Central Processing Unit
    c. Input Devices
    d. Output Unit

22. A computer comprises how many types of memory?
    a. One
    b. Four
    c. Three
    d. Two

23. Which of the following are the physical parts of a computer?
    a. Software
    b. Operating System
    c. Software Applications
    d. Hardware

24. A _____ is a transmission path, made of a set of conducting wires over which data or information in the form of electric signals, is passed from one component to another in a computer
    a. Bus
    b. Path
    c. Medium
    d. system

25. The _____carries the address location of the data or instruction.
    a. address bus
    b. Data bus
    c. system bus
    d. control bus
26. The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____
    a. Set associative
    b. Associative
    c. Direct
    d. Indirect
27. While using the direct mapping technique, in a 16 bit system the higher order 5 bits are used for _____
    a. Tag
    b. Block
    c. Word
    d. Id
28. In associative mapping, in a 16 bit system the tag field has _____ bits.
    a. 12
    b. 8
    c. 9
    d. 10
29. LRU stands for _____
    a. Low Rate Usage
    b. Least Rate Usage
    c. Least Recently Used
    d. Low Required Usage
30. When the data at a location in cache is different from the data located in the main memory, the cache is called _____
    a. Unique
    b. Inconsistent
    c. Variable
    d. Fault
31. In _____ mapping, the data can be mapped anywhere in the Cache Memory.
    a. Associative
    b. Direct
    c. Set Associative
    d. Indirect
32. What is computer organization?
    a. structure and behaviour of a computer system as observed by the user
    b. structure of a computer system as observed by the developer
    c. structure and behaviour of a computer system as observed by the developer
    d. structure specify the functioning, organisation, and implementation of computer systems
33. _____field specifies the operation to be performed like addition, subtraction multiplication etc.
    a. Address field
    b. Operand field
    c. Opcode field

d. Mode field

34. _____ algorithm replaces the page that has not been referred by the CPU for the longest time.
    a. FIFO
    b. LIFO
    c. LRU
    d. OPTIMAL PAGE

35. The performance of cache memory is frequently measured in terms of a quantity called

    a. Miss ratio
    b. Hit ratio
    c. Latency ratio
    d. Read ratio

36. Which of the following is equal to 4 bits?
    a. Byte
    b. Nibble
    c. Record
    d. word

37. What does EEPROM stands for?
    a. Electrically Erasable and Programmable Read-Only Memory
    b. Electronically Erasable and Programmable Read-Only Memory
    c. Electrically Enabled and Programmable Read-Only Memory
    d. Electronically Enabled and Programmable Read-only Memory

38. The last on the hierarchy scale of memory devices is _____
    a. Main memory
    b. Secondary memory
    c. TLB
    d. Flash drives

39. When power is switched off which memory loses its data?
    a. Non-Volatile Memory
    b. Volatile Memory
    c. Interleaved memory
    d. coherent memory

40. The chip by which both the operation of read and write is performed _____
    a. RAM
    b. ROM
    c. PROM
    d. EPROM

41. _____is also known as the computer system's main memory that communicates directly within the CPU.
    a. Secondary memory
    b. Buffer memory
    c. Virtual memory
    d. Primary memory

42. _____, the most significant bits of the memory address decides memory banks where a particular location resides.
    a. Low order memory interleaving
    b. high order memory interleaving
    c. Mid order memory interleaving
    d. Memory order interleaving
43. _____is the combination of opcode and operand that can be used to instruct a system.
    a. Instruction format
    b. Instruction set
    c. Instruction
    d. Data
44. _____Uses first byte to specify the operation i.e opcode and second byte to specify the operand
    a. 3-byte instructions
    b. 2 bytes instructions
    c. One byte instruction
    d. Zero-byte instruction
45. The result of operation is stored in the _____ register
    a. Memory
    b. Buffer
    c. Accumulator
    d. Control
46. The addressing mode, where you directly specify the operand value is _____
    a. Immediate
    b. Direct
    c. Definite
    d. Relative
47. _____Enable the machine-or assembly language programmer to minimize main memory references by optimizing use of registers.
    a. User-visible registers
    b. control register
    c. status register
    d. data register
48. In a Microprocessor, the address of the new next instruction to be executed is stored in
    a. Stack pointer
    b. address latch
    c. Program counter
    d. General purpose register
49. The _____ holds the contents of the accessed memory word.
    a. MAR
    b. MBR
    c. PC
    d. IR
50. _____are the instructions which perform basic operations such as AND, OR, etc
    a. Arithmetic Instructions

b. Logical instructions
c. Data transfer instructions
d. Register instructions

51. If the control signals are generated by combinational logic, then they are generated by a type of _____ controlled unit.
    a. Micro programmed
    b. Software
    c. Logic
    d. Hardwired
52. CD-ROM stands for _____
    a. Compactable Read Only Memory.
    b. Compact Data Read Only Memory.
    c. Compactable Disk Read Only Memory.
    d. Compact Disk Read Only Memory

53. To execute an instruction or program CPU perform various operations step by step and these instructions are commanded by the control unit of the CPU is called as

    a. Nano operation
    b. Numa operation
    c. Micro operation
    d. Control coperation
54. In the _____both cache and main memory are updated with every write operation.
    a. write-through policy
    b. write-back policy
    c. write buffer
    d. write inside

55. If a set has n blocks, the cache placement is then called

    a. 2-way set distributive
    b. 2-way set associative
    c. n-way setting
    d. n-way set associative
56. Which of the following memory technology is highly denser?
    a. DRAM
    b. SRAM
    c. EPROM
    d. Flash memory
57. Which of the following computer memory is fastest?
    a. Register
    b. Hard disk
    c. RAM
    d. SRAM
58. Which of the following memory of the computer is used to speed up the computer processing?
    a. Cache memory

b. RAM
c. ROM
d. Hard Disk

59. Which of the following circuit is used to store one bit of data?
    a. Flip Flop
    b. Decoder
    c. Encoder
    d. Register
60. Which of the following is a way in which the components of a computer are connected to each other?
    a. Computer parts
    b. Computer architecture
    c. Computer hardware
    d. Computer Software
61. Which of the following memory unit communicates directly with the CPU?
    a. Auxiliary memory
    b. Main memory
    c. Secondary memory
    d. Virtual Memory
62. Since, ROM has the capability to read the information only then also it has been designed, why?
    a. For controlling purpose
    b. For loading purpose
    c. For booting purpose
    d. For erasing purpose
63. The CISC stands for _____
    a. Computer Instruction Set Compliment
    b. Complete Instruction Set Compliment
    c. Computer Indexed Set Components
    d. Complex Instruction set computer
64. An _____reads consecutive instructions from memory while in the other segments the previous instructions are being implemented.
    a. instruction pipeline
    b. instruction formatting
    c. instruction sequencing
    d. instruction fetching
65. CMA is a_____
    a. Data transfer instruction
    b. Logical instruction
    c. Arithmetic instruction
    d. Register instruction
66. For adding operands immediately _____ instruction used.
    a. ADD
    b. ADC
    c. ADI
    d. ADP
67. Which operation are associated with serial transfer of data:

a. Logical micro-operation
b. Arithmetic micro-operation
c. Shift micro-operation
d. Data micro-operation

68. What kind of a flag is the sign flag?
    a. General Purpose
    b. Status
    c. Address
    d. Instruction
69. Execution of several activities at the same time.
    a. processing
    b. parallel processing
    c. serial processing
    d. multitasking
70. _____is a measure of how many of the operations in a computer program can be performed simultaneously.
    a. Bit level parallelism
    b. Instruction-level parallelism (ILP)
    c. Data level parallelism
    d. Task level Parallelism
71. Instruction execution involves five phases which are:
    a. Fetch, decode, operand, fetch, Execution, results.
    b. Operand fetch, fetch, decode, Execution, results.
    c. Fetch, execute, decode, operand fetch, results.
    d. Fetch, decode, result, operand fetch, execution
72. A _____is defined as as statement which is true if some condition is satisfied and false if that condition is not satisfied .
    a. logic statement
    b. instruction statement
    c. Decoding statement
    d. Fetching statement
73. The AND operator represent _____
    a. logical multiplication
    b. logical subtraction
    c. logical addition
    d. logical division
74. In negative logic A _____level represents logic 1 A _____level represents logic 0
    a. low voltage, high voltage
    b. high voltage ,low voltage
    c. low voltage low voltage
    d. high voltage ,high voltage
75. Instructions are executed sequentially, and the system may or may not have internal parallel processing capabilities are called as
    a. SIMD
    b. MISD

c. MIMD
d. SISD

76. Array Processors are put under which of these categories:
    a. SISD
    b. SIMD
    c. MISD
    d. MIND
77. Which of the following is independent of the address bus?
    a. Secondary memory
    b. Main memory
    c. Onboard memory
    d. Cache memory
78. Multiprocessing _____
    a. Make the operating system simpler
    b. Allows multiple processes to run simultaneously
    c. Is completely understood by all major computer vendors
    d. Allows the same computer to have the multiple processors
79. Which multiprocessor system contains a master slave relationship?
    a. Symmetric Multiprocessors
    b. Singleton Multiprocessors
    c. Asymmetric Multiprocessors
    d. Flynn's multiprocessor
80. Use of computer buses to connect different components of computer is known as
    a. bus interconnection
    b. layout of computer components
    c. computer structure
    d. bus topology
81. Which of the following is not one of the interconnection structures?
    a. crossbar switch
    b. hypercube system
    c. single port memory
    d. time-shared common bus
82. When an instruction is read from the memory, it is called
    a. Memory Read cycle
    b. Fetch cycle
    c. Instruction cycle
    d. Memory write cycle
83. _____ is a command given to a computer to perform a specified operation on some given data:
    a. An instruction
    b. Command
    c. Code
    d. Program
84. A flag in which the total number of 1s in a valid (n+1) bit code word is even, this is called an _____:

a. Even parity code
b. Odd parity code
c. encoded parity code
d. Decoded parity code

85. The initial stage for an instruction executing in pipelining is -----?
    a. Decode
    b. Execute
    c. Fetch
    d. Address generation.
86. How many types of Pipelining exist?
    a. 2
    b. 3
    c. 4
    d. 5
87. The Control unit of a computer _____
    a. Stores data in the memory
    b. Accepts input data from the keyboard
    c. generates control signals to execute an instruction
    d. generates outputs
88. The 1's complement of a binary number is obtained by changing
    a. each 1 to 0
    b. each 0 to 1
    c. each 1 to 0 and each 0 to 1
    d. no changes in bits
89. What is the addition of the binary numbers 11011011010 and 010100101?
    a. 0111001000
    b. 1100110110
    c. 11101111111
    d. 10011010011
90. The set of loosely connected computers are called as _____
    a. LAN
    b. WAN
    c. Workstation
    d. Cluster
91. One input many outputs is termed as____

    e. Comparator
    f. Multiplexer
    g. Inverter
    h. Demultiplexer
92. In a combinational circuit, the output at any time depends only on the _____ at that time.
    a. Voltage
    b. Intermediate values
    c. Input values
    d. Clock pulses

93. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____
    a. Combinational circuits
    b. Sequential circuits
    c. Latches
    d. Flip-flops
94. The flip flops are categorized into _____
    a. One
    b. Two
    c. Three
    d. Four
95. In a multiprocessor system, data inconsistency may occur among adjacent levels or within the same level of the memory hierarchy is called as_____
    a. Cache interleaving
    b. Cache coherence
    c. Cache miss
    d. Cache hit
96. NUMA stands for
    a. New uniform memory access
    b. Non-uniform memory access
    c. Nand uniform memory access
    d. Note uniform memory access
97. Which of the following register can interact with the secondary storage?
    a. PC
    b. MAR
    c. MDR
    d. IR
98. In which of the following form the computer stores its data in memory?
    a. Hexadecimal form
    b. Octal form
    c. Binary form
    d. Decimal form
99. PROM stands for _____
    a. Programmable Read Only Memory
    b. Pre-fed Read Only Memory
    c. Pre-required Read Only Memory
    d. Programmed Read Only Memory
100. _____ a binary code that indicates the operation to be performed is called as an opcode
    a. Opcode
    b. Operands
    c. Instruction
    d. Program